ABSTRACT OF THE DISCLOSURE

A semiconductor memory comprises, a data memory having a plurality of memory regions to store data at addresses specified, a code memory having the same address space as the data memory to store error correction codes, an error correction code control circuit including an error correction code generation circuit, a syndrome generation circuit and an error correction code decoding circuit, generating an error correction code for correcting data before the data is written back into the memory region, and comparing the generated error correction code with corresponding error correction code, thereby to determine whether the data is erroneous, and an error correction code function invalidity control circuit invalidating an error correction function of the error correction code control circuit when the memory regions are accessed first after power application.